CLAIMS:

1. An amplifier circuit comprising:

a driver stage having at least a first active device which receives a signal for pre-amplification and outputs a pre-amplified signal;

a phase shifter which adjusts a phase of said pre-amplified signal and outputs a phase-shifted signal;

an output stage having at least a second active device which receives said phase-shifted signal for further amplification and output of an amplified signal;

a detector which measures levels of forward signal and reflected signal of said amplified signal; and

a control circuit which controls said phase shifter in response to said levels of forward signal and reflected signal to substantially maintain linearity of said amplifier circuit with load variations.

2. The amplifier circuit of claim 1, wherein said output stage is coupled to a load without an isolation device between said output stage and said load.

3. The amplifier circuit of claim 1, wherein said control circuit modifies a gain of at least one of said at least first active device and said at least second active device to substantially maintain said linearity of said amplifier circuit with said load variations.

4. The amplifier circuit of claim 1, wherein said control circuit independently controls said at least first active device and said at least second active device.

5. The amplifier circuit of claim 1, wherein said control circuit independently controls said phase shifter, said at least first active device and said at least second active device to substantially maintain said linearity of said amplifier circuit with said load variations.

6. The amplifier circuit of claim 1, wherein said at least first active device and said at least second active device are NPN transistors.

7. The amplifier circuit of claim 1, further comprising an input match circuit coupled between an input of said amplifier circuit and said driver stage for matching an input impedance of said amplifier circuit to an output impedance of a device coupled to said input.

8. The amplifier circuit of claim 7, further comprising at least one capacitor coupled between said input match circuit and said driver stage.

9. The amplifier circuit of claim 1, further comprising at least one capacitor coupled between an input of said amplifier circuit and said driver stage.

10. The amplifier circuit of claim 1, further comprising an inter-stage match circuit coupled between an output of said driver stage and an input of said phase shifter.

11. The amplifier circuit of claim 10, further comprising at least one capacitor coupled between said phase shifter and said output stage.

12. The amplifier circuit of claim 1, further comprising at least one capacitor coupled between said phase shifter and said output stage.

13. A wireless communication device comprising the amplifier circuit of claim 1.

14. An amplifier circuit comprising:

a driver stage having at least a first active device which receives a signal for pre-amplification and outputs a pre-amplified signal;

a phase shifter which adjusts a phase of said pre-amplified signal and outputs a phase-shifted signal;

an output stage having at least a second active device which receives said phase-shifted signal for further amplification and output of an amplified signal;

a detector which measures levels of forward signal and reflected signal of said amplified signal; and

a control circuit which independently and selectively controls switching said phase shifter, said at least first active device, and said at least second active device as a function of said levels of forward signal and reflected signal to substantially maintain linearity of said amplifier circuit with load variations.

15. A method for substantially maintaining linearity of an amplifier circuit with variations of a load coupled to an output of said amplifier circuit comprising:

measuring levels of forward signal and reflected signal at said output; and

modifying a phase shifter to change a phase of an output signal of said amplifier circuit as a function of said levels to substantially maintain linearity of said amplifier circuit with load variations.

16. The method of claim 15, wherein said modifying act further modifies a first gain of a first active device of a driver stage, and a second gain of a second active device of an output stage of said amplifier circuit in response to said levels to substantially maintain said linearity.

17. The method of claim 16, wherein said modifying act independently and selectively modifies said phase shifter, said first gain and a second gain.